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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,573	06/29/2001	Yoshio Hagihara	15162/03810	7850

24367 7590 09/08/2003

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EXAMINER
ALLEN, STEPHONE B

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 09/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/896,573	HAGIHARA, YOSHIO	
	Examiner	Art Unit	
	Stephone B. Allen	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

Applicant's arguments filed 12 June 2003, concerning claims 1-23, have been fully considered but they are not persuasive.

Examiner appreciates applicant's summary of the invention and arguments. However, the examiner must respectfully disagree. Firstly, applicant argues (page 7, 2nd paragraph) that both Shinotsuka and Dhuse fail to disclose a pixel that includes "a RAM, a ROM or the like, a comparator, and a calculation device". However, the claims fail to recite these features as well. Secondly, Shinotsuka and Dhuse teach correction for fixed pattern noise FPN in an output image signal. Shinotsuka discloses a log pixel-MOS sensor that outputs data used to correct for noise in an output current caused by a 1st pixel. Dhuse also teaches correction for FPN using 2nd pixel data to compensate the pixel data, as claimed. Therefore, it would have been obvious for one of ordinary skill in the art to modify the imager of Shinotsuka, as taught by Dhuse, to compensate a 1st pixel data with a 2nd pixel data. Thus, the examiner must respectfully disagree with applicant's assertion that the rejection is not obvious and further must assert that Shinotsuka and Dhuse teach all of the claimed limitations as explained in the following rejection.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinotsuka in view of Dhuse.

Regarding claims 1-3, 13 and 16: Shinotsuka shows in Figure 1 a solid-state image-sensing device comprising a plurality of pixels 4 including a photoelectric conversion element and capable of generating an output signal that is logarithmically proportional to an amount of light incident on the photoelectric conversion element. Also disclosed in Figure 4 is correction circuitry 6 which operates to provide a compensation signal for compensating the output signal of the pixels, reducing signal noise that is caused by the first pixel (see Col. 2, lines 25-39), as well as reading circuits 2,3 for reading out the output signals of the first and second pixels (see Col. 4, lines 31-40). Shinotsuka does not specifically teach the compensation circuitry as provided in the form of second pixels disposed in the main array. However, it is well known in solid-state image-sensing devices having a plurality of pixels to designate 1st pixels for generating an output signal and a plurality of 2nd pixels for generating a signal to be used to compensate for unwanted aspects of the first pixel signals. Figure 5 of Dhuse shows a solid-state image-sensing device which comprises 1st pixels 502A-502N,506A-506N,510A-510N for generating an output signal, and 2nd pixels 400, 516,518 used as reference pixels for deriving an adjustment value to compensate for unwanted noise aspects obtained in the first pixel signals (see Col. 6, lines 65-67 and Col. 7, lines 1-9 and 21-36). It would have been obvious to one of ordinary skill in the art at the time that the invention was made to provide the correction circuitry 6 of Shinotsuka in the form of a pixel, and to dispose this 2nd pixel in the array of original pixels 4, in order to

consolidate the compensation and output signal elements rather that separating them, which would require mores space. Also, by designating separate, 2nd pixels to obtain a correction signal value, the correction signals applied to the 1st pixels would not be biased by problems inherent to the 1st output signal pixels.

Regarding claim 4: The modified solid-state image-sensing device of Shinotsuka teaches the 1st pixels (e.g. 4, Shinotsuka, Figure 1) as arranged in a two-dimensional array, and the 2nd pixels (e.g. reference pixels 400,516,518, Figure 5, Dhuse) arranged in a line in such a way to correspond one-to-one to *rows* of the 1st pixels. This configuration does not expressly disclose the 2nd pixels as provided in a line in such a way as to correspond one-to-one to *columns* if the 1st pixels. However, this would only involve rearrangement of these components. And it has been held that rearranging parts of an invention involves only routing skill in the art. *In re Japikse*, 86 USPQ 70.

Regarding claim 5: The modified device of Shinotsuka comprises output signal lines provided, one for each column, permitting the output signals of the first and second pixels arranged in an identical column to be extracted therethrough (see column driver circuit 3, Figure 1, and Col. 4, lines 37-40).

With respect to claim 6: The modified device of Shinotsuka does not expressly disclose the 2nd pixels as being smaller in size than the 1st pixels, but it would have been obvious to configure them in this manner, in order to minimize the space taken by the compensation pixels and allow the maximum area for obtaining signals to be provided to the 1st signal generating pixels. Also, a change in size is generally

recognized as being with the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPa1955).

Regarding claim 7: The 1st and 2nd pixels in the modified device of Shinotsuka inherently have different circuit configuration since one pixel performs signal output and on performs compensation.

Regarding claim 8: As disclosed in Shinotsuka, the 1st pixels 4 of the modified device include a photoelectric conversion element PD (see Figure 2), and the 2nd pixels, corresponding to the correction device 6 of Figures 4 and 5, include no photoelectric conversion elements.

Regarding claim 9: The modified device of Shinotsuka does not specifically teach the 1st and 2nd pixels, corresponding to the pixel having the photoelectric conversion element and the pixel generating the compensation signal, as having an identical circuit configuration. However, it would have been obvious to one of ordinary skill in the art to arrange both types of pixels, or all pixels in the image-sensing device, to have identical circuitry (therefore each comprising photoelectric conversion components and also compensation means), in order to provide the ability to selectively designate certain pixels of the array as compensation pixels and certain pixels as active illumination-sensitive pixels, rather than being limited to an arrangement of permanently fixed roles in corresponding sections of the array.

Regarding claim 10: The modified device of Shinotsuka does not specifically teach the 1st and 2nd pixels as receiving different voltages (see pixel-cell architecture of Shinotsuka, Figure 1, and Dhuse, Figures 2 and 4). However, it would have been

obvious for one of ordinary skill in the art to have configured the device to provide separate voltages to the 1st and 2nd pixels. This arrangement would prevent voltage fluctuations or errors in either the signal-outputting or compensating pixels from affecting the other respective pixel and therefor the compensation adjustments.

Regarding claim 11: The 1st and 2nd pixels of the modified device of Shinotsuka each include a plurality of MOS transistors Q1,Q2,Q3 included in the pixel cell architecture (see Fig. 2).

Regarding claims 12 and 15: As shown in Figure 3 of Shinotsuka, the output voltage of the pixel 4 remains linear until point Y, at which a higher illumination level is sufficient to produce a change to logarithmic output voltage behavior. The modified device of Shinotsuka can therefore selectively generate either a linear or logarithmic output signal, depending upon the illumination provided to the photodiode (e.g. PD, Figure 2). It would have been obvious to also include in the modified device an optical shutter or filter which is selectively placeable over photodiode PD of the pixels, in order to regulate the amount of light entering this device and therefore the output voltage generated for controlling the type of output (linear or logarithmic) produced.

Regarding claim 14: The modified device of Shinotsuka shows in Figures 4 and 5 the compensation circuitry 6 as including a storage circuit 7 for storing the output signal of the second pixel (signal for compensation). It also shows a data comparator for comparing the pixel signal with correction data values (see Col. 7, lines 9-18). It does not specifically teach the use of a differential amplifier circuit for outputting a difference between the output signal of the 1st pixel and the output signal of the 2nd pixel

stored in the storage circuit. However, the setup shown by Figures 4 and 5 of Shinotsuka is functionally equivalent in terms of analyzing a signal obtained by 1st pixels with compensation values, and it would have been obvious to implement a differential amplifier for this purpose, in order to compare compensation and signal data and provide an amplified signal for adjustment and read-out purposes.

Regarding claim 17: Figure 16 of Shinotsuka shows the device as comprising a memory (storage devices 21,22 within section 20) for storing the 2nd pixel output signal, as well as for storing compensation data (see Col. 8, lin3e 8 – Col. 9, line 39(.

Regarding claims 18-20: Although Shinotsuka discloses that the signal noise caused by the 1st pixel is associated with the output signal of the pixel, it does not specifically teach this noise as being the result of a switching action of a semiconductor device in the system, or more specifically, the result of a transistor being turned off or the 1st pixel being reset. However, it is well known in the art to compensate for noise created by such actions or components, as taught by Dhuse. The reference/compensation pixels in Dhuse are used "to eliminate the noise which is generated by the reset of the photodiode" signals of active pixels (Col. 2, lines 20-22, see also Col. 7, lines 20-35). It would have been obvious for one of ordinary skill in the art to compensate through such means for the noise created by the reset of a pixel in Shinotsuka, or the activation or deactivation of a transistor or any other device in the system, in order to counter any unwanted noised created by the operation and output of active pixels.

Regarding claim 21: Though not specifically stated in the present claimed invention, the 2nd pixels must also be read out by the reading circuit to compensate for the variations (noise) in the signal. Therefore, the modified Shinotsuka does read out the 1st pixels and the 2nd pixels compensates for variation of the signal from the reading circuit.

Regarding claim 22: Shinotsuka fails to disclose that the characteristic is an amplification factor. Since it is known to amplify signals prior to readout to insure that the strength of the signal is at a desired level. It would be obvious for one of ordinary skill in the art to modify the 2nd pixel to include compensation for amplification variations, to ensure accuracy in the signal output.

Regarding claim 23: The modified Shinotsuka does not specifically disclose that the reading circuit is a transistor and that the characteristic is an amplification factor. It is well known to use transistors as readout device as shown in Dhuse. It would have been obvious for one of ordinary to include such in the reading circuit of Shinotsuka.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephone B. Allen whose telephone number is (703) 308-4828. The examiner can normally be reached on Mon-Thurs from 0900-1700.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Porta can be reached on (703) 308-4852. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Stephone B. Allen
Primary Examiner
Art Unit 2878

sba